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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,233	11/19/2001	Yvon Gris	S1022/8800	8198

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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1722	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,233	GRIS ET AL.	
	Examiner	Art Unit	
	Matthew J. Song	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,13,15,20-24,26-32,36,37,39-41 and 45-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,13,15,20-24,26-32,36,37,39-41 and 45-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 11, 13-15, 21-24, 26-30, 32, 36-37, 39-41, and 45-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa et al (US 5,734,195) in view of Meyerson (US 5,298,452) and further in view of Tihanyi et al (US 3,897,625) or Takiyama et al (JP 8-8262), an English Abstract has been provided.

Takizawa et al discloses a Si substrate **11** grown a Czochralski method is dry oxidized at a temperature of 1000°C to form a SiO_2 film **13** on the surface of the substrate **11**. Takizawa et al also discloses carbon is ion-implanted into the substrate through the SiO_2 film **13** and the resultant structure is annealed in an N_2 atmosphere. Thereafter, the SiO_2 film is removed and a Si

epitaxial layer **16** is grown at a temperature of about 1150°C (col 4, ln 15-65). Takizawa et al also discloses ion-implanting electrically neutral C, Ge, Sn, Pb or the like which are Group IV elements may be ion-implanted into the Silicon substrate **11** and an element other than a Group IV element may be ion-implanted into the substrate together with the Group IV element (col 6, ln 15-35). Takizawa et al also teaches annealing is not necessarily required depending on an acceleration or dose at which the carbon is ion-implanted (col 5, ln 1-5), this reads on applicants' depositing a silicon layer on the region prior to annealing the substrate since annealing does not need to be performed. Omission of a step and its function is held to be obvious (MPEP 2144.04).

Takizawa et al does not disclose depositing a silicon layer on the region at a temperature of less than 750°C.

Meyerson teaches a method of forming epitaxial silicon using silane and a hydrogen carrier gas at a growth temperature of less than 800°C at a pressure of 10^{-2} to 10^{-4} Torr (1.3 to 0.013 Pa). Meyerson also teaches excellent uniformity is obtained across the wafer because of the low pressure (col 9, ln 9-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Takizawa et al with Meyerson process of forming epitaxial silicon at reduced temperatures to form an epitaxial silicon layer with excellent uniformity at reduced operating temperatures and superior properties (col 17, ln 20-35).

The combination of Takizawa et al and Meyerson does not teach forming a window in a layer on the substrate to expose the region.

In a method of selective gettering, note entire reference, Tihanyi et al teaches making a field effect transistor having a short channel length by forming a protective covering layer on a silicon layer that can be gettered, removing portions of the protective layer and forming a

gettering layer on the exposed silicon surface (Abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al and Meyerson with Tihanyi et al selective gettering using a protective layer to form a useful field effect transistor device.

In a method of manufacturing a semiconductor device, Takiyama et al teaches using silicon nitride film as a mask to form and implanting carbon to form gettering sites in a silicon substrate (Abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al and Meyerson with Takiyama et al mask so as to gettering in a selective manner, thereby forming a useful semiconductor device.

Referring to claims 13-15, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches silane and hydrogen at a pressure of 1.3 Pa and 50 Torr.

Referring to claims 21, 24, 39 and 41, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches removing an oxide layer and a thickness of 20 nm. The combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama does not teach a thickness of less then 10 nm and depth of 5 nm or less. The combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches the thickness of SiO_2 film can be reduced depending on the acceleration or dose of the implantation ('195 col 5, ln 1-5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al, Meyerson and Tihanyi

et al or the combination of Takizawa et al, Meyerson and Takiyama by using an oxide thickness of less then 10 nm for a reduced implantation dose.

Referring to claim 22, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches ion-implantation, this reads on applicants' process that directs ions toward the region.

Referring to claims 23 and 40, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama does not teach the density of interstitial defects. The combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama does teach crystal defects form in the substrate by implantation improve the gettering capability of the wafer ('195 col 6, ln 5-15), this is a teaching that the defects are result effective variables. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama by conducting routine experimentation to determine the optimum amount of interstitial defects per one hundred silicon atoms.

Referring to claim 26, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama et al is silent to the width of the window. The dimensions of a mask are well known in the art to be directly related to characteristic features of the semiconductor device produced and smaller devices are well known to be advantageous. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al, Meyerson and Tihanyi

et al or the combination of Takizawa et al, Meyerson and Takiyama et al by optimizing the width of the protective layer by conducting routine experimentation (MPEP 2144.05).

Referring to claims 27 and 32, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama is silent to the silicon layer is deposited with a different orientation than that of the substrate. However, since the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches a similar method as claimed, under the principle of inherency the invention is considered to be anticipated by the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama.

Referring to claim 29, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama is silent to the crystallinity of the substrate. However, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches a substrate formed by the Czochralski process. The Czochralski process inherently produces substrate with single crystalline orientation, as evidenced by Matsuo et al (US 4,515,755) below.

Referring to claim 30, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama inherently teach a single crystalline silicon substrate, as discussed previously; therefore an epitaxial silicon grown on a single crystalline substrate will inherently be single crystalline.

Referring to claim 45-46, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama does not teach the pressure. The combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al,

Meyerson and Takiyama teach pressures from 50 Torr to 1 atm. Overlapping ranges are held to be obvious (MPEP 2144.05). Furthermore, pressure is well known to be a result effective variable. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama by optimizing pressure by conducting routine experimentation of a result effective variable (MPEP 2144.05).

Referring to claims 49-50, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches carbon, this reads on applicants' atoms.

Referring to claims 47-48 and 51-52, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches a temperature of less then 800°C, specifically 550°C. Overlapping ranges are held to be obvious (MPEP 2144.05).

3. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa et al (US 5,734,195) in view of Meyerson (US 5,298,452) and further in view of Tihanyi et al (US 3,897,625) or Takiyama et al (JP 8-8262), an English Abstract has been provided, as applied to claims 11, 13-15, 21-24, 26-30, 32, 36-37, 39-41, and 45-52 above, and further in view of Wu et al (US 4,584,026).

The combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches using electrically neutral elements into a silicon

substrate. The combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama does not teach using fluorine.

In a method of ion-implantation of phosphorus, arsenic or boron, note entire reference, Wu et al teaches implanting fluorine ions and then implanting phosphorus, arsenic or boron because double implanted wafers reached a useful level of conductivity at lower temperatures (col 5, ln 1-30). Wu et al also teaches fluorine ions are electrically inert (col 3, ln 20-30 and col 4, ln 5-20), this reads on applicants' implanting electrically neutral species and this is a teaching that fluorine is acceptable as an electrically neutral species. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama with Wu et al's fluorine implant because substitution of a known material based on its suitability is held to be obvious (MPEP 2144.07).

4. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa et al (US 5,734,195) in view of Meyerson (US 5,298,452) and further in view of Tihanyi et al (US 3,897,625) or Takiyama et al (JP 8-8262), an English Abstract has been provided, as applied to claims 11, 13-15, 21-24, 26-30, 32, 36-37, 39-41, and 45-52 above, and further in view of Candelaria (US 5,441,901).

The combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama teaches all of the limitations of claim 11, as discussed previously, except the region comprises an emitter of a bipolar transistor.

In a method of making a semiconductor device, Candelaria teaches a silicon semiconductor layer forms an emitter region in a heterojunction bipolar transistor device (claim 1; col 2, ln 20-45 and col 4, ln 40-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the silicon layer taught by the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama by forming an emitter to be useful in a semiconductor device, as taught by Candelaria.

Response to Arguments

5. Applicant's arguments, see page 8 of the remarks, filed 5/2/2005, with respect to Kagata have been fully considered and are persuasive. The rejection of 11, 13-15, 20-24, 26-32, 36-37, 39-41, and 45-52 has been withdrawn. Kagata teaches annealing prior to epitaxial deposition.

6. Applicant's arguments filed 5/2/2005 have been fully considered but they are not persuasive.

Applicant's argument that one of ordinary skill in the art would have been motivated to modify Takizawa process to include the step of deposition a silicon layer at a temperature of less than 750°C is noted but is not found persuasive. Applicant alleges that a lower epitaxial growth temperature would reduce gettering capability and one of ordinary skill would not sacrifice gettering capability of the resulting wafer. Takizawa teaches the cooling step for increasing a gettering effect and oxygen precipitation is more accelerated when a second element is implanted into a substrate (col 3, ln 30-50) and oxygen is precipitated at 650°C (col 1, ln 50-65). The lower epitaxial deposition process by Meyerson would be expected to produce the desired results because oxygen precipitates a lower temperature and cooling results in increased gettering.

Furthermore, a person of ordinary skill in the art would have been motivated to form an epitaxial layer with excellent uniformity, as taught by Meyerson.

Applicant's argument that Tihanyi and Takiyama do not teach forming a window is noted but is not found persuasive. Tihanyi teaches a mask is applied over a predetermined area to protect parts of the silicon surface from a getter process (col 2, ln 15-25) and Takiyama teaches using a silicon nitride film as a mask, which reads on applicant's window because a window by definition merely means an opening and clearly removing portions of a mask will form opening.

Applicant's argument that claim 32 is patentable is noted but is not found persuasive. The Examiner admits the prior art does not teach the silicon layer has a different crystalline orientation than the substrate and maintains that the feature is inherent. The instantly claimed invention achieves the different orientation by implantation to cause damage to the substrate and then performing epitaxial deposition. The prior art teaches ion implantation and epitaxial deposition; therefore since a similar process is performed, a similar result is expected. Also, the ion implantation causes defects to the surface of the substrate ('195 col 2, ln 20-50). The majority of the substrate is undamaged and would retain its original orientation, while the surface, which the epitaxial deposition occurred would be slightly different from the original orientation because of the implantation process. Therefore, different implanation would not result in inherent differences, as suggest by applicant, because defects would still be cause regardless of implant energies.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Plumton (US 5,554,561) teaches that doping by implantation affects the crystal orientation of GaAs grown on GaAs (col 1, ln 60-67 and col 7, 50-67).

Burns et al (US 5,011,789) teaches growing a single crystal Si film at 650-800°C at a pressure of 6 Pa and the importance of low temperatures to prevent transfer of dopants (col 3, ln 35 to col 4, ln 15 and col 6, ln 1-5).

Matsuo et al (US 4,515,755) teaches a well known method of manufacture of silicon single crystals used as wafers for semiconductor devices is the Czochralski method (col 1, ln 5-40).

Mochizuki et al (JP 2-044714) teaches ion-implanting germanium into a silicon single crystal substrate and depositing a silicon thereon followed by annealing the film (Abstract).

Kurogi et al (US 4,637,127) teaches a silicon single crystal substrate used in CMOS (col 11, ln 10-20).

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

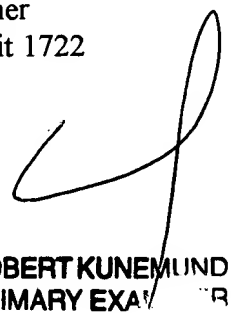
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duane Smith can be reached on 571-272-1166. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1722

MJS
July 9, 2005



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